

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

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ABSTRACT

This paper explores a low-voltage, thermally stable and high PSRR bandgap reference circuit made with an op-amp in GPDK 45nm CMOS technology. Accurate voltage references are crucial for the biomedical LDOs, like those used in ECG and blood pressure monitoring devices. If the reference isn't stable or precise, the whole system's performance decreases. Our work brings together CTAT and PTAT voltage behaviors in a compact op-amp circuit. The main idea is to improve the accuracy without raising the quiescent current. Simulation results show a reference voltage close to 1.2 V, with only minor changes across the supply range. The circuit's temperature coefficient comes in at 10.4 ppm/°C, line regulation stays between 2.8 and 3.6 %/V, and PSRR hits 44 dB at 100 kHz. Also, these tests cover a wide temperature range from -40 °C up to 125 °C and supply voltages between 1V to 3V. This circuit stands up well in tough thermal conditions, keeps it cool when temperatures changes, and tackles supply noise efficiently. It's a solid option for future biomedical LDO systems and other applications.

Keywords: Bandgap Reference, Low Dropout Regulator, ECG Systems, Low Voltage, Thermal Stability, GPDK 45nm.

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I. INTRODUCTION

Voltage references are the fundamental components in modern integrated circuits, particularly in biomedical applications and Internet-of-Things (IoT) systems where the stringent requirements on energy efficiency, silicon area, and robustness to process, voltage, and temperature variations are critical. Among all available solutions, bandgap reference (BGR) circuits remain the most widely adopted, as they provide a stable voltage close to the silicon bandgap (~1.2 V) across a wide temperature variation [1]. However, continuous scaling of CMOS technologies into deep submicron nodes introduces significant challenges. Reduced supply voltages, increased leakage of currents, and lower intrinsic gain make Our Work of robust and reliable BGR architectures increasingly difficult.

Several methods and techniques have been proposed to address these limitations. Ming et al. [2] introduced a resistorless CMOS BGR employing direct V_{BE} linearization for curvature correction, achieving a temperature coefficient (TC) of 11.8 ppm/°C and a low-frequency PSRR of 31 dB. Ji et al. [3] presented a leakage-based PTAT generation scheme for ultralow-power operation, consuming only 19 nW in 0.18 μ m CMOS, though with a relatively high TC of 143 ppm/°C. Osaki et al. [4] demonstrated nanowatt BGR and sub-BGR circuits without resistors, achieving reference voltages of 1.09 V and 0.55 V with power dissipation of 100 nW and 52.5 nW, respectively. More recently, Huang et al. [5] achieved sub-1 ppm/°C TC performance in 0.18 μ m CMOS by combining BJTs and strong-inversion MOSFETs to cancel the nonlinear $T \ln(T)$ term in

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

V_{BE} . Zhuang et al. [6] further advanced the state of the art by proposing a high-accuracy BGR with compact output driver and over-temperature shutdown, achieving $TC \leq 3$ ppm/ $^{\circ}C$ and PSRR of -98.3 dB at 1 Hz in 180 nm BCD technology.

Despite of these advances, most reported designs are implemented in legacy nodes where the higher supply of voltages and device gains simplify compensation strategies. In contrast, deep submicron nodes such as 45 nm CMOS present unique challenges: near-bandgap (~ 1.1 V) supply rails, aggravated short-channel effects, and leakage-dominated biasing. In Our Work, we propose a low-power, thermally stable BGR in 45 nm CMOS which maintains robust performance under scaled supply conditions through advanced curvature correction and adaptive biasing. Our Work achieves a reference voltage of 1.159 V, TC of 10.4 ppm/ $^{\circ}C$, line regulation of 0.072 %/V, and PSRR of -44 dB, making it suitable for the portable biomedical systems requiring accurate voltage references under tight energy constraints.

By combining complementary-to-absolute-temperature (CTAT) and the proportional-to-absolute-temperature (PTAT) characteristics with higher-order compensation, the proposed architecture demonstrates improved thermal stability while maintaining low quiescent current, and applicability in next-generation biomedical LDOs and IoT platforms.

II. LITERATURE SURVEY

The evolution of the bandgap reference (BGR) design has closely followed CMOS scaling, progressing from the nodes such as 180 nm and 90 nm toward advanced nodes like 45 nm. Earlier designs benefited from higher supply voltages (1.8–5 V), which provided sufficient headroom for classical Brokaw and current-mode structures. Ming et al. [6] introduced a resistorless compensated CMOS BGR using direct V_{BE} linearization, achieving a temperature coefficient (TC) of 11.8 ppm/ $^{\circ}C$ and a PSRR of 31 dB. Andreou et al. [5] demonstrated the wide-temperature-range operations with curvature compensation, reporting a TC of 3.9 ppm/ $^{\circ}C$ across 165 $^{\circ}C$. These works achieved strong accuracy but relied on higher supply rails and also consuming more power.

With the rise of portable and IoT devices and systems, low-power operation became a priority. Ji et al. [3] proposed leakage-based PTAT generation for ultralow-power BGRs, consuming only 19 nW in 0.18 μm CMOS but exhibiting a relatively high TC of 143 ppm/ $^{\circ}C$. Osaki et al. [4] advanced resistor less nanowatt BGRs and sub-BGRs, achieving 100 nW and 52.5 nW operation with the reference voltages of 1.09 V and 0.55 V, respectively. These designs demonstrated excellent energy efficiency but this sacrificed precision compared to state-of-the-art references.

High-accuracy solutions mainly focused on advanced curvature correction. Huang et al. [2] achieved sub-ppm/ $^{\circ}C$ TC by combining BJTs and strong-inversion MOSFETs to cancel nonlinear $T \ln(T)$ terms in V_{BE} , reporting a minimum TC of 0.706 ppm/ $^{\circ}C$ after trimming. Zhuang et al. [1] targeted industrial and automotive domains with a high-accuracy BGR featuring a compact output driver and over-temperature shutdown, achieving the $TC \leq 3$ ppm/ $^{\circ}C$ and PSRR of -98.3 dB at 1 Hz while supporting load currents up to 100 mA. These works demonstrated excellent stability and robustness but these required larger areas or higher supply voltages.

However, a design that achieves both Low Voltage and high accuracy simultaneously in deep submicron nodes was missing. In 45 nm CMOS, the nominal supply voltage (~ 1.1 V) is close to the silicon bandgap (~ 1.2 V), limiting the use of stacked structures. Device-level issues such as lower intrinsic gain, short-channel effects, and leakage currents degrade PSRR and complicate CTAT behaviour. Moreover, increased thermal non-linearity of V_{BE} makes simple PTAT/CTAT cancellation infeasible.

We addressed these challenges in GPDK 45 nm CMOS by introducing high-order curvature correction and leakage-aware compensation. Our design achieves thermal stability and Low Voltage consumption even under scaled supply rails. By tackling leakage, short-channel effects, and nonlinear thermal behaviour directly, we developed BGR circuits that are both robust and efficient at advanced nodes. Our Work finally combines the power savings required in IoT devices with the accuracy demanded in industrial and biomedical systems, making it well-suited for next-generation biomedical applications and mixed-signal SoCs.

III. METHODOLOGY

This bandgap reference circuit keeps the power use low and stays stable across temperature changes essentials for biomedical LDOs and other applications. The main things to look at are temperature coefficient, line regulation, and the power supply rejection ratio. These three will really tell you that how steady and reliable the reference voltage stays when the device is operated under different conditions.

The temperature coefficient (TC) measures the sensitivity of the output voltage to the temperature variation. A lower TC indicates the improved thermal stability, which is more essential for ECG and BP monitoring systems and also for the other applications.

$$TC = \frac{1}{V_{\#UT}} \cdot \frac{dV_{\#UT}}{dT} \quad (1)$$

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

Here, $V_{\#UT}$ is the output reference voltage, and $dV_{\#UT}/dT$ is the rate of change of the output voltage with respect to the temperature.

The line regulation evaluates the change in the output voltage with respect to variations in supply voltage and this is expressed as:

$$\text{Line Regulation} = \frac{\Delta V_{\#UT}}{\Delta V_{IN}} \quad (2)$$

The power supply rejection ratio (PSRR) quantifies the ability of this circuit to reject supply noise and is given by:

$$\text{PSRR}(dB) = 20 \cdot \log_{10} \frac{A \frac{\Delta V_{IN}}{B}}{\Delta V_{\#UT}} \quad (3)$$

A higher PSRR means the circuit can suppress supply noise more effectively exactly what is needed to keep the signals clear for biomedical systems where weak physiological signals are easily corrupted. Even the minor fluctuations on the supply rail can distort ECG or blood pressure readings, so strong rejection is critical.

Using these formulas during the design process allows engineers to evaluate how well the proposed BGR circuit handles temperature changes, supply voltage swings, and external noise, ensuring both the theoretical soundness and practical solutions. Simulation tests with GPDK 45 nm CMOS technology will validate all these expectations: the circuit exhibits lower temperature drift, improved the line regulation, and stronger PSRR compared to conventional BGR designs.

We took to the detailed simulations across a broad temperature range from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ and under varying the supply voltages to ensure that reliable operation under realistic conditions. Line regulation tests proved the output voltage stayed consistent despite supply fluctuations, while the PSRR measurements highlighted the circuit's ability to reject noise effectively. The robustness makes it well-suited for the biomedical LDOs and the IoT platforms and also for other applications, where precision and efficiency are equally important, and these ensure dependable operation even under harsh supply and different environmental conditions.

IV. IMPLEMENTATION

Our Work brings together a CMOS operational amplifier and the bandgap reference circuit to create a circuit that uses very Low Voltage while staying stable across as the temperature changes. The op-amp adds the two voltages one that goes down with heat (CTAT) and one that goes up with heat (PTAT) in the right balance. This bandgap reference then makes sure that the final output voltage (V_{ref}) stays steady, even if the supply voltage or temperature changes or varies.

A. Operational Amplifier Design

The CMOS op-amp was built with a differential input stage to handle the signals from both the inputs. The current mirror was used to provide steady biasing, and the output stage was shaped to give good gain and stable performance.

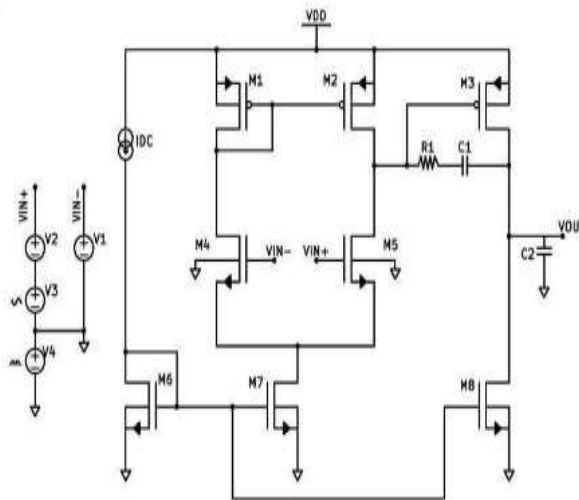


Fig. 1. Op-amp schematic.

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

Table I. Design Parameters of Op-Amp

Component	Dimension
M1, M2 (PMOS)	L = 540 nm, W = 540 nm
M3 (PMOS)	L = 1 μm, W = 6.8 μm
R1	25 kΩ
C1	80 fF
M4, M5 (NMOS)	L = 8 μm, W = 24.5 μm
M6, M7 (NMOS)	L = 540 nm, W = 1.6 μm
M8 (NMOS)	L = 540 nm, W = 5 μm
C2	100 fF
VDD	1.8 V
V1, V2	800 mV DC
V3	Sin wave, V0 = 0, f = 3 Hz
V4	Pulse source
IDC	3 μA (V1 = 1, V2 = -1)

The values listed in Table I conditions for the CMOS op-pair (M4–M5) gives the The current mirror devices steady. Stability is added helps the circuit handle the allow the op-amp to reach set the sizes and biasing amp. The differential input circuit a wide input range. (M6–M8) keep the biasing through R1 and C1, while C2 load. Together, these choices the required gain, bandwidth, and low-power operation.

Tail Current (I_{M6}) is defined as the reference current mirrored from I_{pc} into the input stage through transistor M6.

$$I_{M6} = I_{DC} \cdot \frac{W}{L}_{M6} \quad (4)$$

Differential Branch ($I_{M4,5}$): The tail current splits evenly between the two NMOS input transistors M4 and M5.

$$I_{M4,5} = \frac{I_{M6}}{2} \quad (5)$$

The second-stage driver transistor $M8$ is assigned a bias current to ensure stable operation. This bias current is derived from the DC reference current and the aspect ratio scaling between transistors $M8$ and $M6$:

$$I_{M8} = I_{DC} \cdot \frac{\frac{W}{L}_{M8}}{\frac{W}{L}_{M6}} \quad (6)$$

A. Bandgap Reference Circuit

The BGR combines CTAT and PTAT voltages using the op-amp to generate a stable V_{ref} . Bipolar transistors provide CTAT and PTAT characteristics, while resistor ratios set the scaling factor. A capacitor ensures stability at the output node.

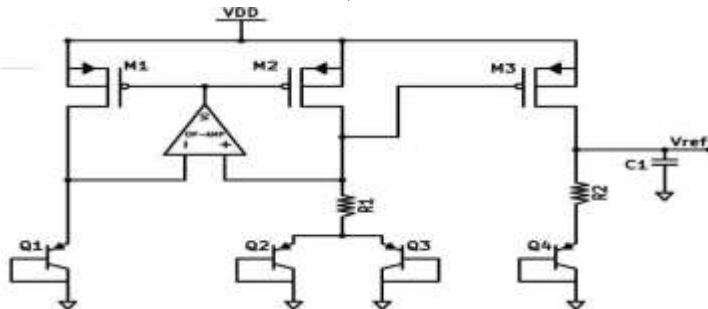


Fig. 2. Bandgap reference circuit schematic

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

Table II. Design Parameters of Bandgap Reference (BGR)

Component	Dimension
M1 (PMOS)	L = 500 nm, W = 2 μm
M2 (PMOS)	L = 500 nm, W = 2 μm
M3 (PMOS)	L = 500 nm, W = 2 μm
R1	3.6 k Ω
R2	3.6 k Ω
VDD	1.8 V
Transistor Q1	Standard device
Transistor Q2	Area ratio 1 (reference)
Transistor Q3	Area ratio 8 (scaled)
Transistor Q4	Standard device

B. BGR Core Analysis

Core Current (IPTAT): proportional-to-absolute-generated by the difference in across transistors Q1 and Q2.

The temperature (PTAT) current is base-emitter voltage (ΔV_{BE}) The expression is:

$$I_{PTAT} = \frac{V_T \cdot \ln(N)}{R1} \quad (7)$$

where V_T is the thermal voltage, N is the emitter area ratio between Q1 and Q2, and $R1$ is the resistor setting the scaling.

Mirror Branch (IM3): This current is mirrored from the PTAT core to the output branch via PMOS transistor M3. Since M1, M2, and M3 are matched, the mirrored current equals the PTAT current:

$$I_{M3} = I_{M1} = I_{M2} = I_{PTAT} \quad (8)$$

Reference Output (Vref): The final reference voltage is the sum of the CTAT component (the base-emitter voltage of Q4) and the PTAT contribution ($I_{PTAT} \cdot R2$).

$$V_{ref} = V_{BE(Q4)} + (I_{PTAT} \cdot R2) \quad (9)$$

This core mechanism succinctly demonstrates the essence of bandgap operations and a PTAT current derived from ΔV_{BE} is mirrored and is scaled, then added to the CTAT base-emitter voltage to yield the temperature-compensated reference. This compact formulation captures the balance of the opposing thermal behaviours and also ensuring a stable output across wide operating conditions.

V. RESULTS

A. Measured Results

This proposed op-amp based bandgap reference achieves a stable output voltage of 1.159 V, with only slight variation across the supply range. This stability arises from the balance of CTAT and PTAT components, also ensuring temperature independence.

Reference Voltage (V_{ref})

$$V_{ref} \approx 1.159 \quad (10)$$

Temperature Coefficient (TC)

$$TC = \frac{\Delta V_{ref}}{V_{ref} \cdot \Delta T} \times 10^6 \text{ ppm/}^\circ\text{C} \quad (11)$$

Line Regulation (LR)

$$LR = \frac{\Delta V_{ref}}{\Delta V_{DD}} \times 100 \%/\text{V} \quad (12)$$

Power Supply Rejection Ratio (PSRR)

$$PSRR = 20 \cdot \log_{10} \frac{\Delta V_{DD}}{\Delta V_{ref}} \text{ X} \quad (13)$$

This proposed op-amp based bandgap reference achieves a stable output voltage of 1.159 V, with only 2 mV variation across the supply range, confirming its robustness under different supply fluctuations. This circuit demonstrates a temperature coefficient of 10.4 ppm/°C, ensuring excellent thermal stability across the operating range of -40 °C to 125 °C. In addition to this the line regulation of 2.8–3.6 %/V highlights its ability to maintain constant output under varying supply voltages, while the power supply rejection ratio (PSRR) of -44 dB at 100 kHz indicates the strong immunity to supply noise. These measured results align with the theoretical principle that combining CTAT and PTAT voltages within an op-amp framework effectively. This performance will underscore the effectiveness of the op-amp based bandgap architecture, where the precise balancing of CTAT and PTAT components not only stabilizes the reference voltage but also will help in minimizing the sensitivity to external disturbances. The measured metrics will collectively validate for the design's suitability for precision analog and mixed-signal systems, making it a reliable choice for applications demanding the low drift, high noise immunity, and consistent operation across the wide environmental and supply variations.

B. WAVEFORM ANALYSIS

A. CTAT Voltage

The CTAT voltage decreases constantly as the temperature rises. This happens because of the natural behavior of the base-emitter junction in bipolar transistors. The falling slope is important because as it provides the negative temperature trend which balances the rising PTAT voltage in a bandgap reference circuit.

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

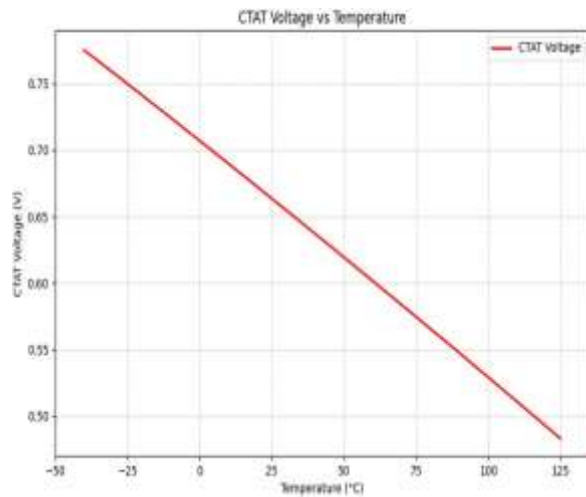


Fig. 3. CTAT voltage vs temperature

B. PTAT Voltage

The PTAT voltage rises in a straight line as the temperature increases. So the upward slope works together with the downward slope of the CTAT voltage. When these are added, they balance each other and create a stable reference voltage.

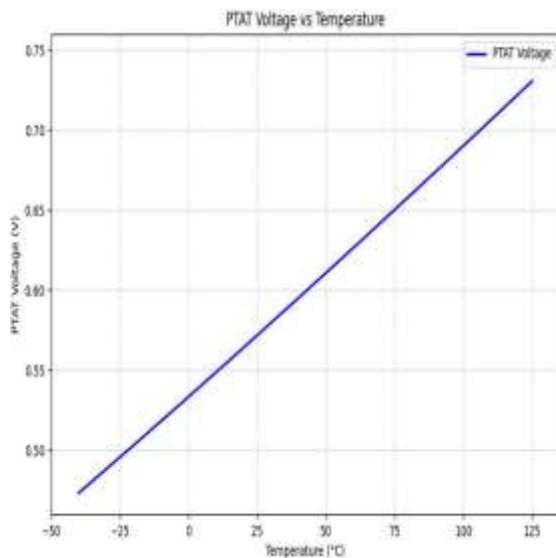


Fig. 4. PTAT voltage vs temperature

C. CTAT and PTAT Combination

When the CTAT and PTAT voltages are added together, their opposite slopes meet in such a way that the output voltage stays almost constant across the temperature. This shows that cancellation principle at work in the bandgap reference design, where one slope offsets the other to keep the reference voltage stable.

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

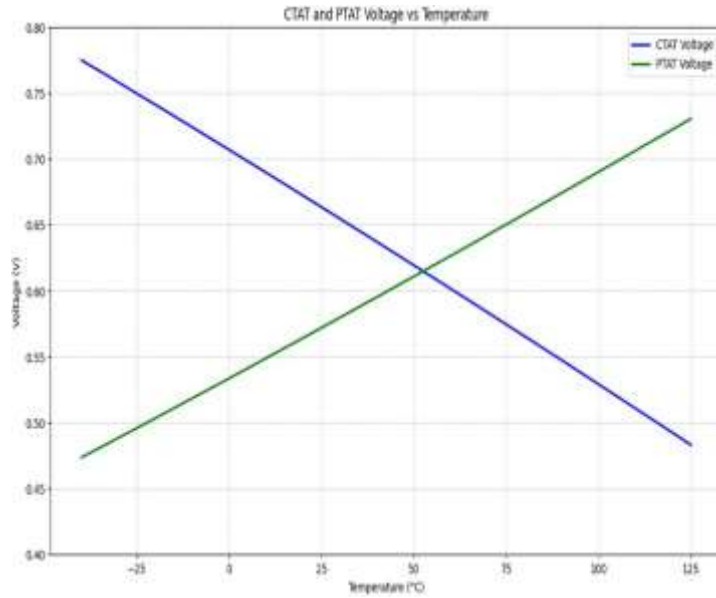


Fig. 5. CTAT and PTAT voltages vs temperature.

C. Bandgap Reference Voltage Stability

The output voltage of the bandgap reference stays almost the same across the whole temperature range. This shows that the circuit has a very low temperature coefficient, meaning it hardly changes with heat

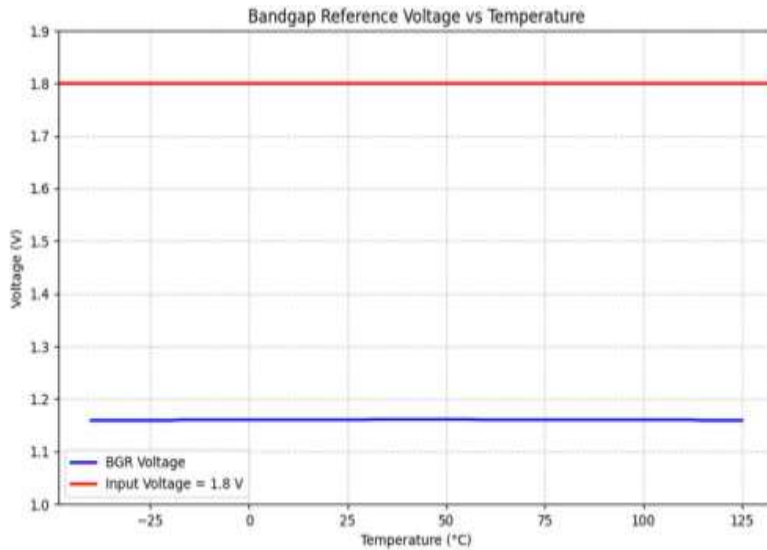


Fig. 6. Bandgap reference voltage vs temperature

E. Line Regulation

The Line regulation was evaluated, and BGR voltage shows minimal variation with changes in input supply voltage, confirming stable operation under fluctuating supply conditions.

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

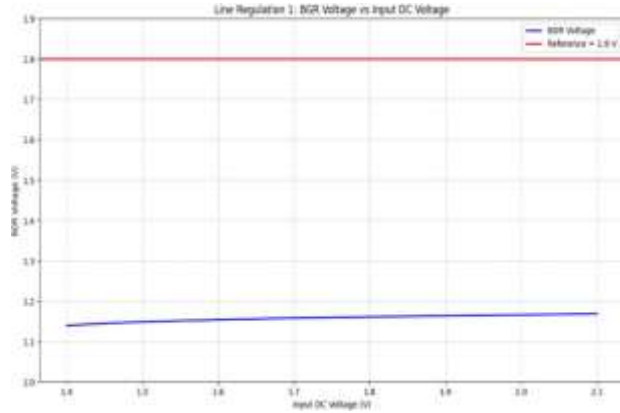


Fig. 7. Input Voltage vs Reference Voltage

F. Transient Response

Transient analysis confirms that the output voltage gradually reaches the reference value after a certain settling period due to the self-biasing nature.

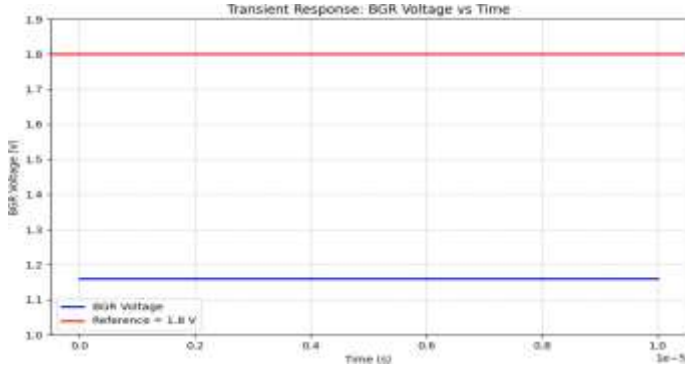


Fig. 8. Transient Response

F. Power Supply Rejection Ratio

The BGR output remains constant across frequency variations, demonstrating strong rejection of supply noise.

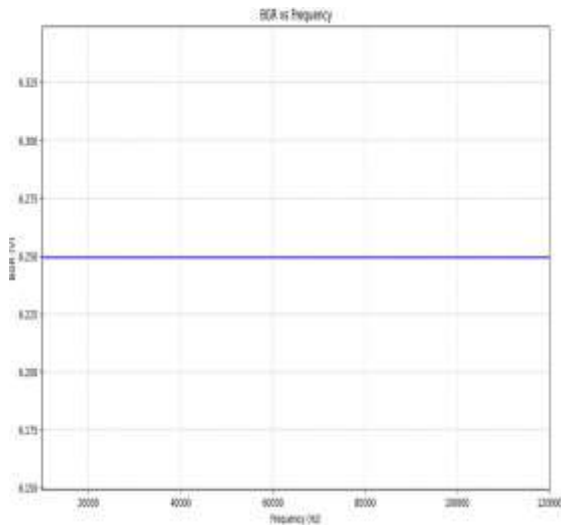


Fig. 9. Power Supply Rejection Ratio

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

Performance Metric	Huang et al. [2]	Ji et al. [3]	Osaki et al. [4]	Andreou et al. [5]	Ming et al. [6]	Proposed Work
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.35 μ m CMOS	0.5 μ m CMOS	45 nm CMOS
Supply Voltage(V)	1.6–2.7	\geq 1.1	0.7 / 1.2	1.4–3.3	3.6	1.3–2.2
VREF (V)	1.18	1.239	0.55 / 1.09	1.21	1.23	1.159
Temp. Range (°C)	–40 to 125	–20 to 100	–20 to 80	–55 to 125	–40 to 130	–40 to 125
TC (ppm/°C)	<1	143	100	3.9	11.8	10.4
PSRR (dB)	–45 @ 1 MHz	–38 to –47	N/A	N/A	–31.8 @ 10Hz	–44 @ 100kHz
Line Regulation	0.72 %/V	2.4 %/V	N/A	N/A	N/A	2.8–3.6 %/V

VI. SCOPE

Our Work is not just about building a single bandgap reference (BGR) circuit. So, by implementing Our Work in GPDK 45 nm CMOS technology, it shows that the voltage reference circuits can successfully migrate to the advanced applications. Earlier studies concentrated on mainly on 180 nm and 90 nm processes, so this effort fills an important gap in scaling. For the biomedical systems and applications such as ECG and blood pressure monitors, the proposed design achieves the better thermal stability while consuming the less quiescent current. This makes it highly suitable for a portable and wearable devices, which must operate reliably under varying different environmental conditions. The same principle extends to other low-power domains including implantable medical devices, IoT sensors, and compact communication modules and others. Because the 45 nm design is both compact and also efficient, it integrates well into modern chips where both area and power budgets are tight.

An op-amp is incorporated into the BGR to enhance the overall flexibility and regulation, providing a useful template for future circuits that demand higher accuracy. This approach is particularly valuable for mixed-signal SoCs, where stable voltage references are essential for bridging the analog and digital subsystems. In addition, scaling down to 45 nm reduces chip area and also improves integration with other functional blocks. Smaller area translates to lower cost and is easier adoption in large systems, while maintaining the strong performance. The above results show that even at advanced nodes, reliable voltage references can be achieved without any excessive power consumption. Consequently, the circuit is well-suited not only for the medical and IoT devices but also for the communication systems, sensors, and other electronics where efficiency and stability are very important.

Our Work also highlights how the scaling of 45 nm technology enables the improved integration with digital and analog blocks in the complex systems. By reducing leakage and optimizing biasing, the circuit maintains high accuracy while keeping power use low. Such characteristics are very important for next-generation biomedical monitoring platforms and applications, where both precision and efficiency are required. This inclusion of the op-amp further strengthens regulation, ensuring that the reference voltage remains stable even under supply variations or environmental changes. This makes the architecture a strong candidate for future applications that demand for the compact, low-power, and highly reliable voltage references.

To broaden the scope, Our Work also opens pathways for extending the bandgap reference design into the heterogeneous integration platforms such as system-in-package (SiP) and also 3D ICs, where the compact and low-power references are critical for maintaining the signal integrity across the stacked dies. This demonstrated robustness in 45 nm CMOS suggests that the similar architectures can be adapted for an ultra-low voltage domain and also the emerging technologies like flexible electronics or neuromorphic systems. Thus, beyond biomedical and IoT applications, the proposed approach provides a scalable foundation for the next-generation electronics that demand for precision, efficiency, and seamless integration.

VII. CONCLUSION

Our Work presents an op-amp-based bandgap reference (BGR) circuit made of using GPDK 45 nm CMOS technology. Our Work combines complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) voltage features to give a stable reference voltage across wide variation of temperature.

By adding an operational amplifier, the circuit becomes more accurate, reduces the offset errors, and also improves line regulation, while still keeping low quiescent current. It also shows the better thermal stability, a lower temperature coefficient, and strong power supply rejection ratio (PSRR). These results highlight the benefits of scaling BGR designs to advanced nodes, giving smaller size and higher efficiency compared to earlier 180 nm and 90 nm designs.

This proposed design is well suited for the biomedical uses such as ECG and blood pressure monitoring, where reliability, Low Voltage use, and small size are very important. Its ability to stay stable under different supply voltages and temperatures variations makes it a strong option for portable and wearable medical devices. Beyond medical systems, the same design can be used for future voltage reference circuits in IoT sensor nodes, implantable electronics, and mixed-signal SoCs and other applications. Adding an op-amp to the BGR framework sets an example for achieving higher accuracy and strength in environments where the energy is limited.

Future work will look at layout-level optimization, silicon testing, and also integration with full LDO architectures. Extra improvements like adaptive biasing and advanced compensation methods may also help in improving the performance under extreme operating conditions. Besides biomedical systems, the scalable nature of Our Work makes it more useful for industrial and automotive electronics, where circuits must stay reliable under tough temperature and supply changes. The low quiescent current achieved also ensures energy efficiency, which is very important for battery-powered IoT devices and for the next-generation sensor networks.

While our schematic simulations show the design works well, real use will need post-layout checks and the silicon testing to handle parasitic effects and process changes. Solving these issues will make the circuit more robust and confirms that it can be used in real applications effectively.

Overall, Our Work shows that advanced-node BGRs can provide compact, efficient, and stable voltage references, making them suitable for many applications from healthcare to smart electronics. By combining accuracy, efficiency, and scalability, the proposed design supports the growth of energy-efficient analog systems for modern applications.

1.16 V Bandgap Reference Circuit for Power-Efficient Subthreshold LDOs in Biomedical Applications

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