A LOW POWER 14T SRAM USING SELF-RESILIENCE RADIATION-HARDENED TECHNIQUE FOR AEROSPACE APPLICATION

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ABSTRACT
Although these deep micron storage devices are sensitive to soft errors such as single event upset (SEU) and double node upset (DNU), they play an important role in space electronics. During a node upset, space ions are hitting a scaled memory circuit and causing loss of the critical charge in sensitive memory nodes across all nodes in the array. This study delineates the RHBD-14T soft fault immune SRAM cell for applications such as satellites and space travel. The SEI-14T memory cell consists of two latch circuits which are coupled in a self-recovering, state-correcting feedback arrangement. The relative performance of the SEI-14T is shown via a comparison with other advanced radiation-resistant memory cells, such as the RHM-12T, RHD-12T, RSP14T, and RH-14T. Compared to the other cells with memory referred to herein, SEI-14T shows remarkable writing stability and outstanding read stability. We used Tanner EDA version 16.1 for the simulations & schematics.
Keywords: Radiation Hardening, Critical Charge, Ion Track, Double Node Upset (DNU), Single Events Upset, Soft Errors.
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I. INTRODUCTION

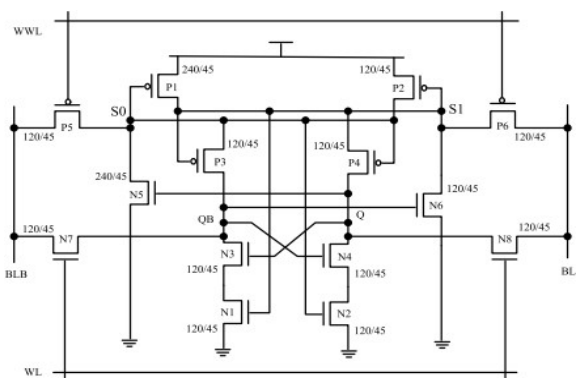
Static memory with random access (SRAM) is a key feature of system-on-a-chip (SOC) and contributes significantly to the electrical power consumption and area of the SOC. Because the district is crucial to the design of the circuit. In conventional 6T or 8T cells, they will only work on smaller sections because they are not designed to handle larger sections. The bit-line move causes a data subordination break and a reduced □□□/□□□□ percentage, due to the fact that it reads other cells in one section. Hence, to solve this problem, new circuits are needed. Until now, the methods of solving this problem have been based on obtaining, and keeping, an ION/IOFF ratio that allowed parts up to 1kg. There are still lots of people who don't grasp the basic concept of the energy function of SRAMs, and as a result, lose a lot of power when they do high volts per association. This research features three types of SRAM bit cell with NMOS-only read ports: they minimize the read port leakage due to RBL, enhance intelligence, reduce the size and power consumption of the conventional 6T and 8T cells, and current understanding cells. SRAM's impact has grown with the proliferation of small battery-powered devices and low limits sensors. The major goals of SRAM development have been to increase yield to be able to scale voltage. The conventional 6 transistor (6T) cell, which has a thick profile, and bit connection and is able to be differentiated and detected well, is not the most ideal cell for reading and writing in static random access memory (SRAM). This complements earlier work, which has overcome similar challenges through the use of aid tactics, unique cell topologies, targeted upgrades and new discoveries. Responding to SRAMs' read-troublesome and half-choice problems, the word-line voltage rate plan was developed. Copy control transistors and process corner observers can be handled with the aid of the data line sub drive.

By matching the inward voltage of the half-selected cells' bit lines with the assistance of the cellular supply boost and by delaying the word line increase a little bit during reading cycles, while using the driving force of the NMOS pull, the stability during read or write cycle could be fine-tuned. Negative cellular deployment is the best way to improve readability, but if many GND rails are used, there are high energy costs.

II. LITERATURE REVIEW

The core of a typical 6T SRAM cell consists of 2 pairs of cross coupled inverters and two pairs of n-type MOS (NMOS) entry control gate transistors (ECGT) connect the 2 bit lines BL and BLB to each other. The overall design of the cell is simple and compact. The traditional 6T SRAM (transistor) cell has severe read/write conflicts since it shares the same path for both operations. The standard 6T SRAM cell has low read static noisy margin (RSNM)/write serial noise margin (WSNM) at severe low-supply voltage (Golipour, 2021), as an indication of read stability/writability. There are two metrics that compete in the design of the standard 6T SRAM cell: RSNM and WSNM. Hence, it is very difficult to use the 6T SRAM cell under critically low-supply voltage due to below the semiconductor transistor threshold voltage. The basic SRAM cell (8T SRAM) is proposed in (L. Chang, 2005) to remove the read disturbance of the 6T SRAM cell. Compared to the traditional 6T SRAM cell, the isolated read route of an 8T SRAM cell is created by two extra NMOS access transistors, one read word line and a read bit line. To enhance the performance of RSNM, the data storage nodes are totally separated from the data reading bit line during the reading operation. However, in scaled technology, the single read path

leakage is very significant and this cell is affected by it. An improvement of as much as 30% area has been observed, even with just a 30% increase in area. In (Kulkarni, 2011), the read stability problems were solved using the basic concept of Schmitt-Trigger (ST). In this study, the authors have proposed two types of ST based SRAM cells to improve the stability of the cells. The feedback process has some disadvantages, as it will only work while the voltage of the storage nodes is being held; if the voltage on the storage nodes starts to dissipate or charge, the feedback process is not effective in the ST1 bit cell. The feedback mechanism can only be useful, if the voltage at the storage nodes is maintained constant. This restriction is eliminated by projecting the ST2 SRAM cell. To enhance the feedback system, a distinct control signal is utilised. With this differential sensing technique, two independent word lines (WL and WWL) and two independent bit lines (BL and BLB) have been used. The area overhead of this bit cell is larger than other read/write assist systems, yet is suitable for low voltage operations. (Sanvale, 2019) projects and displays a PMOS-PMOS-NMOS cell core 10T (PPN10T) SRAM cell. A differential writing structure is used for writing and a single-ended reading structure is used for reading. By employing a differential writing path and an isolated read path, this cell is able to enhance RSNM/WSNM. This cell has a stacked transistors in its core, which reduces the power dissipation from leakage. The high dynamic write energy use is caused by its dual terminated write bit lines, though. In (Ensan, 2018), a robust cell called feedback reducing 11T FinFET SRAM cell (FC11T) is proposed. The FC11T SRAM cell consumes less power when writing and reading as both write and read operations use only one bit line. This cell can be used to improve RSNM and WSNM with the help of the isolated reading path and the feedback-cutting write-assist techniques, respectively. These enhancements will result in lower reading and writing speeds. For operations close to the subthreshold, this cell is determined to be resilient. To improve the RSNM and WSNM and reduce the power consumption, (Ahmad, 2016) proposes another SRAM cell with 11 transistors (ST11T). The read decoupling approach, the virtual grounded write assistance technique and the single-ended structure result in an increase of the RSNM, the WSNM, or the power consumption, respectively. However, this cell have the same isolated reading path to the conventional 8T SRAM cell, and show greater leakage in this direction. The 45nm technologically designed area is doubled than the 6T SRAM cell. Using single-ended reading & differential writing architectures, (Tomar, 2020) discusses a ST-inspired 12T (ST12T) SRAM cell. This cell uses the power gating write-assist scheme, and suffers from read disturbance but has high WSNM. By using a single-ended reading operation, this cell can enhance the dynamic reads power consumption. Nevertheless, the area overhead is an issue for this cell.



III. SRAM CELL DESIGN 14T SRAM CELL

More optimisation is needed for 12T SRAM. A 14T SRAM cell, designed to improve power consumption and write latency, was thus developed. Now, the circuit is made up of transmission gates, instead of NMOS pass transistors, which allow the circuit to optimise the high performance attributes of the cell. Analogue transmission gates can handle signals of a wide range of voltages and can switch between two different directions, (Joshika Sharma, 2015). The inability of PMOS and NMOS to pass strong 0s and 1s, respectively, is eliminated. Since both of them conduct at the same time, this issue is solved via transmission gates. It is common practice to use transmission gates in order to decrease the circuit's parasitic resistance and capacitance. This inability may result in reduction of noise margin and more static power dissipation of the circuit according to P. Upadhyay (2014). To activate both transistors, it detects a low sleep transistor signal (ST). A connection between the virtual and real world is thus created. Similarly, in the case of the sleep transistor signal, the virtual supply is linked to the real supply. In the active region, the voltages at the nodes of the transistors are 0 and □□□, respectively, and the transistors are in the linear region. The sleep transistors are turned off to sleep state (P.Upadhyay, 2014), and therefore the subthreshold leakage currents are very small, due to their high threshold. As a result, there will be less loss of power. Both virtual nodes will be in floating mode during the whole changeover process. However, the nodes are connected to weak □□□ then discharged to strong ground as a result of leakage current flowing via the off transistor. When you write 0. In the same way, nodes are charged and discharged. The static power dissipation in the gearbox gate is reduced by the charge recycling mechanism due to the charging and discharging phenomena.

A swing voltage is required when the transistor flips its high and low states at the bit lines. A key component of dynamic power dissipation is it. To keep power loss to a minimum, this has to be cut down. To further decrease dynamic power dissipation at all higher frequencies, our design makes use of two sources of voltage on bit or bit bar lines. The proposed SRAM cell will not only enhance the stability but also possess better switching properties. The Bit Line (BL) is low and the Bit Bar Line (BBL) is high when writing the number 0. To reduce the voltage fluctuation of the output voltage of BBL, NMOS VT2 will be turned ON when NMOS VT1 is turned OFF. This applies also to the letter "1": BL is high and BBL is low. This causes the swing voltage at the bit line output to decrease since VT1 is on and VT2 is off. Despite being larger, the power, latency and stability of this suggested SRAM cell make up for that.

IV. EXISTING SYSTEM

In the method 14T SRAM cell is designed by using CMOS technology and different parameters are calculated.

Fig. 1. Design of Existing 14T SRAM)

V. PROPOSED SYSTEM

A host of charged space particles, such as electrons, alpha particles, or high energy ions not belonging in the Low Earth Orbit zone, threatens the reliability and integrity of memory circuits. Radiation-resistant SRAM chips, such as adding more nodes — the memory cells — that could help restore data that has been corrupted by the particles, which have a disproportionately negative effect on traditional 6T SRAM, are being investigated. In this work, a novel SRAM cell called self resilience radiation- hardened 14T (SRRH-14T) cell is proposed to tackle the soft error problem by introducing redundant nodes.

The recommended SRRH-14T memory performance is comparable to other well known radiation resistant cells such as 6T-SRAM, Quatro 10-T, SEA-14T, RH-14T, QCCS-12T or RRS-14T. The suggested SRRH-14T memory cell safeguards against interruptions caused by many nodes by using a minimally delicate node layout area separation. the thin-cell design of the planned SRRH-14T self-resilience radiation-hardened 14T SRAM cell, and the cell itself. Ten PMOS and four NMOS transistors, two of which are PMOS access transistors, make up the SRRH-14T memory cell. These PMOS transistors connected to the sensitive nodes were many times more susceptible than radiation-hardened transistors. Furthermore, the read stability of the memory cell can be improved by employing PMOS as access transistors for the zeroth line margin [21]. In the proposed SRRH-14T memory cell, the sensitive storage nodes are decreased, since the main storage node I0 or I1 is connected with the same orientation of PMOS transistors. I0 and I1 are like backup storage nodes, I2 and I3 are similar. The fundamental hold, read and write analyses of the SRRH-14T SRAM cell are as follows: A. Analysis of holding In a memory cell with the word line disabled (WL=1), the P2 transistor charges I0 to VDD and the P5 transistor charges I3 to VDD. This implies that I1 can go out through N1 and P6, and I2 can go out through N4 and P6. The same procedure is used for logic 0 stored memory. At this point, the next write or read function will cause both bit lines to be pre-charged to VDD. Figure shows the holding analysis results for the SRRH-14T analysis in logic 1. For read: Worldline activation and VDD supply to both bits is required, precharge is done by sensing amplifier connected to the column array of the memory cell. By allowing BLB to go out via P6 and N1, a voltage difference between BL or BLB will occur because the memory is set to logic 1, as shown in the figure. The sense amplifier then produces a voltage signal corresponding to the sense made by the sense amplifier. Memory cells with a logic 0 also have the bit voltage on the line (VDD) discharged via N2 and P7 transistors. For clarity, the sensory amplifier & precharge were omitted. C. Analyse in Writing Important components of a write operation are write driver or bit lines. When the write driver is driving logic 0 to high logic from a memory cell, BLB is grounded and the bit line is charged to VDD. If P1 and P3 are bypassed, the N1 transistor will turn ON under some circumstances. With the P9 transistor turned on, current flows from I1 to BLB. This will turn N4 transistors ON, and thus turn ON P6, by setting ON conditions for P2 and P4. In Figure ….. the P2 transistor has charged the memory cell to VDD. Specific instructions to enter the 0 (logic) in the cell. A simulation of classic hold, write, & read analysis is shown in figure 5, but is short-lived. D. Analysis of Upset Recovery Data disruptions in places close to low Earth orbit may be caused by high-energy particle hits, which are amplified when an OFF semiconductor drain region becomes linked to the storage node [22]. Consider a PMOS transistor which is turned off, with a logic 0 voltage around the drain region. The situation could impact high energy radiation and cause disturbances due to the additional charge carriers generated by the OFF transistor.

Similarly, the first NMOS OFF outlet will be in logic 0 state after being surrounded with logic 1. The previously proposed 14T SRAM can be constructed from 4 storage nodes. The upset study carried out was for three nodes: I1, I2 and I3 which were found to be sensitive. That I0 is unique to PMOS transistors and takes on the value 1 when storage is also at logic 1 is supported by this relationship. The publications uses a double exponentially current pulse and the proposed SRRH14T is assessed for upset.

VI. SIMULATION RESULTS

Output waveform of 14T SRAM CELL

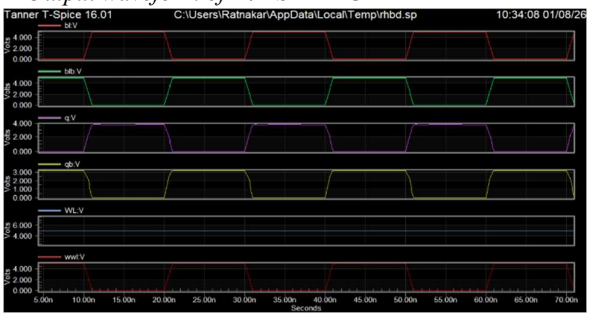


Fig: Simulation Wave Form of Existing 14T Sram.

The waveform of the output of a 14T SRAM cell is shown in fig. 11, where a high word line indicates that the value of the bit line is either 1 or 0, and the output q remains at 1 or 0, respectively. The qbar will also be holding a 1 or 0 when the bitbar is holding one of those values. q and qbar will retain the previously recorded values when the word line is low.

Using Tanner EDA 16.1v, schematics and simulations have been conducted in 25nm CMOS technology. Wave form of a 14-transistor SRAM cell.

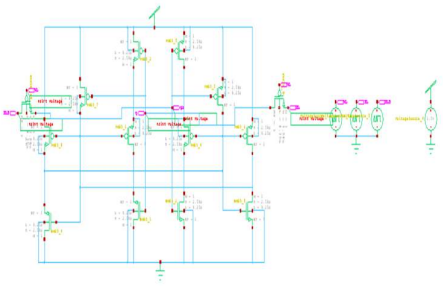


Fig: Design of proposed 14T SRAM

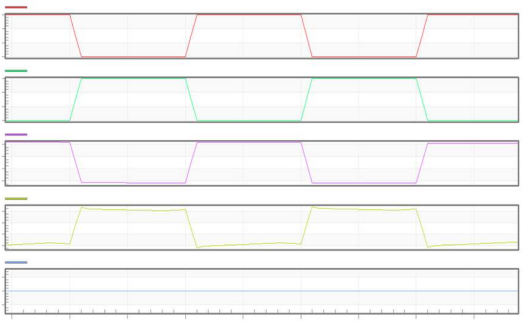


Fig: Simulation Wave Form of Proposed 14T Sram

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Power Results

VVoltageSource_4 from time 0 to 100
Average power consumed -> 2.220275e-013 watts
Max power 2.317057e-004 at time 8.1e-008
Min power 2.123293e-004 at time 1.16648e-008
```

Fig: Power report of proposed 14t sram.

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Parsing                          0.02 seconds
Setup                            0.00 seconds
DC operating point               0.03 seconds
Transient Analysis               0.00 seconds
Overhead                         0.13 seconds
-----------------------------------------
Total                            0.17 seconds
```

Fig: Delay report of proposed 14t sram.

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Device and node counts:
              MOSFETs -      14
    MOSFET geometries -       2
      Voltage sources -       4
          Subcircuits -       0
    Model Definitions -       2
      Computed Models -       2
    Independent nodes -       8
       Boundary nodes -       5
          Total nodes -      13
```

Fig: Area count in proposed 14T SRAM

A variety of charged space particles, in the form of electrons, alpha particles, high-energy ions that are not supposed to be in the Low Earth Orbit zone, threaten the reliability and integrity of memory circuits. Researchers have started to explore radiation resistant SRAM chips, including the possibility of adding extra nodes of memory cells, to restore the corrupted data from such particles which have a disproportionately negative impact on traditional 6T SRAM. In this study, a new SRAM cell, called a self resilience radiation- hardened 14T (SRRH-14T) cell, to resolve the soft error problem is presented.

TABLE I

PERFORMANCE EVALUATION OF EXISTING AND PROPOSED 14T SRAM'S

Parameter	10T SRAM using 25nm CMOS GNRFET	12T SRAM using 25 nm GNRFECT	14T SRAM using 25nm GNRFET	10T SRAM using 18nm CMOS	12T SRAM using 18nm CMOS	14T SRAM using 18nm CMOS	10T SRAM using 16nm FINFET	12T SRAM using 16nm FINFET (adiabatic cell)	14T SRAM using 16nm FINFET (srhbd)
Supply voltage	1v	1v	1v	1v	1v	1v	1v	1v	1V
Average power	1.586763 e-004 Watts	7.142643 e-005 watts	6.755707 e-005 Watts	2.360150 e-005 watts	8.987834 e-005 watts	3.155133 e-005 watts	1.407945 e-004 watts	1.1259997 e-004 Watts	1.1059997 e-004 Watts
Delay	25.0991 Ns	-4.9553 ns	34.9708 ns	20.0803 ns	29.7878 ns	20.0533 ns	24.9669 ns	-4.6417 ns	-3.4417 ns
Output rise time	468.4391 Ps	9.4473 ns	10.3808 ns	9.4659 ns	-39.138 ns	9.4264 ns	-19.266 ns	1.0074 ns	1.0074 ns
Output fall time	9.3755 Ns	-20.408 ns	408.4893 ps	320.9620 ps	29.6206 ns	29.491 ns	15.7162 ns	199.2422 ps	179.2422 ps
Avg power at 70 °C	8.114675 e-005 watts	4.087190 e-005 watts	6.097943 e-005 watts	2.184835 e-005 watts	8.400600 e-005 watts	3.061127 e-005 watts	2.795270 e-004 watts	1.474890 e-004 watts	1.474890 e-004 watts
Avg power at 80 °C	7.252375 e-005 watts	3.770086 e-005 watts	5.959633 e-005 watts	2.145427 e-005 watts	8.303802 e-005 watts	3.046024 e-005 watts	2.973594 e-004 watts	1.527921 e-004 watts	1.427921 e-004 watts
Avg power at 90 °C	6.552963 e-005 watts	3.514399 e-005 watts	5.822997 e-005 watts	2.106157 e-005 watts	8.215993 e-005 watts	3.033648 e-005 watts	3.129233 e-004 watts	1.576419 e-004 watts	1.370419 e-004 watts
Avg power at 100 °C	5.964997 e-005 watts	3.305643 e-005 watts	5.702770 e-005 watts	2.066185 e-005 watts	8.135598 e-005 watts	3.022940 e-005 watts	3.267689 e-004 watts	1.621457 e-004 watts	1.521457 e-004 watts

This 14Tsram was designed using 18nm technology and performance analysis has been carried out and the above results have been achieved by implementing stack technology which increases the performance of the sram in adiabatic approach. The 14t SRAM cell's waveform is similar to the one shown in figure 12, for high values of word line, bit line and output q. If the bitbar contains a 1 or 0, the qbar will also contain the same.

Similarly, an NMOS OFF output will first be surrounded by a logic 1 before it is logic 0. Before is a proposed 14T SRAM consisting of 4 storage nodes (SN). The research on the upset was conducted on three nodes – I1, I2 and I3 – and it was discovered that these nodes are prone to the upset. That I0 is unique to PMOS transistors and takes on the value 1 when storage is also at logic 1 is supported by this relationship. The publications claim 'the proposed SRRH14T is evaluated for upset' by a double exponentially current pulse.

The above comparative table reveals that the values of the Rhbd & Self-Resilience parameters based on 14T SRAM have been improved with respect to the CMOS technology built on 14T SRAM cells.

VII. CONCLUSION AND FUTURE SCOPE

SRAM cell is a robust storage cell that is capable of withstanding high-energy particles hitting one or more nodes in the system; outlined in study is SRRH-14T, a type of SRAM cell. To make it better, we added redundant nodes (two additional nodes with a feedback link) to make data recovery easier if we lose any data. Furthermore, polarisation hardening between the main storage nodes helps to reduce the charge-sharing issue with neighbouring sensitive nodes. In the worst case, the proposed SRRH14T has the least variation in the process and the largest read stability. The proposed cell

is able to reduce read access time and static electrical consumption, and also dynamic electrical consumption significantly, as compared to the above mentioned cells. What is most surprising about this study is that the PVT behaviour is the same with the SRRH-14T, which is able to overcome the charge sharing problem with the same functionality, despite the fact that the PVT shows more critical charge behaviour. In terms of overall performance measure EQM, SRRH-14T memory cell is superior to the existing memory cells. As a result, this SRRH14T is ideal for any memory-related missions in the low orbital Earth area. So, SEI14T series SRAM memory module is a great option for reliable satellite and space applications.

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