RESEARCH PAPER

Low Power Parallel Architectures for LFSR Using State- Space Transformations

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ABSTRACT

Linear feedback shift registers (LFSRs) employ parallel designs for Bose Chaudhuri Hocquenghem (BCH) encoders and cyclic redundancy checks (CRCs). The multi-bit serial and parallel LFSR design is presented in this study. Linear feedback shift registers with effective designs eliminate hold time violations and minimize the feedback loop. Our efficiency metric, the area-time product (A.T.), is defined as (C.P) (XOR + 1.5 D. E.), where 1.5 is the expected ratio of an XOR gate to a delay element in terms of the number of NAND gates. That's because an XOR gate requires four 2-input NAND gates, and a delay element requires six 2-input NAND gates. The better the implementation, the lower the A.T. value. The time product for normalized values in the bottom area indicates the preferred implementations. The building of 32-D flip-flops is necessary for a typical 32-bit LFSR. To achieve 32-bit LFSR capabilities with reduced size, power consumption, and clock route count, 4-bit flip-flops may be used. The Xilinx Vivado Tool examined the setup and hold violations for the 4-bit LFSR. Three timing violations with a slack of
0.269 ns are present for a 4-bit LFSR. Consequently, the experimental data shows that the total on-chip power is growing linearly. For CRC-32, 30% power and 6% gate count savings are achieved.

Index Terms—BCH encoders, linear feed-back shift register, state-space transform matrix, parallel architecture, CRC, low power, generator polynomial.

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INTRODUCTION

Data transmission is done using a Bose Chaudhuri hocquenghem encoder and cyclic redundancy check. The work may be extended to measure the significance of the test patterns generated by the Test Pattern Generator. The feedback loop complexity of a parallel CRC transformation matrix and state-space transform is decreased by parallel designs for linear feedback shift registers (LFSRs). This concept achieves a considerable reduction in power consumption without raising CPD as compared to earlier designs [1]. Further research on the efficient parallel design of LFSR is required. Future research was done in a matrix using the state-space transformation approach. The Xilinx Vivado Tool was used to analyse the setup and hold violations for the 4-bit LFSR. For CRC-32, 30% power and 6% gate count savings are achieved. The superior implementations are shown by the time product for normalized values in the lower area. 32 D flip-flops are needed to design a typical 32-bitsLFSR. Reduced size, power, and clock route count are achieved 4-bits flip-flops to accomplish 32-bit LFSR capability [2],[3]. The same kind of transformations are thoroughly searched for in order to find the transformation that results in the fewest total gate counts [4]. In [5], triangular transformation matrices are used. In a different area of research, the LFSR function is understood as recursive filtering, and recursive filters are processed in parallel [6]. These parallel LFSRs are simpler to construct when the format of the recursive filter changes [7]. In comparison to the state-space transformation, it has more gates. The unfolding approach may also be used to derive parallel LFSRs from serial LFSRs. While their area is bigger. The viable clock frequency can be raised by modifying the divisor polynomial[10] or by including alternative look-ahead pipelining in the crucial loop [8]. We achieve our design by examining several transformations of state-space. My approach begins with the inverse transformation matrix and looks for a matrix that lowers the gate count of the pre-processing matrix multiplication [9]. As opposed to looking for a transformation matrix of a specific format that would reduce the total gate count. The recommended matrix [13],[14],[15] results in fewer nonzero entries in the feedback matrix. For systems employing substructure sharing, a reduced critical path delay (CPD) computation approach is also offered to better assess the logic complexity [16],[17]. The recommended design is based on how many logic gates are in use in the system using the unfolding technique. Although their size is larger, alternative look-ahead pipelining applied to the important loop [18] or divisor polynomial modification [19], can enhance the viable clock frequency. In those that rely on Pre-processing, feedback matrix multiplications and state space transform was require to one clock cycle.

I. PARALLEL LFSR ARCHITECTURES

The arrangement of the serial LFSR represented in figure 1 and given to the generator polynomial $g(x) = x^{n-k} + g_{n-k-1} x^{n-k-1} + \cdots + g_1 x + g_0$. To the division of $u(x)\ x^{n-k}$ by g (x) will

be performed by 4 bits LFSR. When the input with the greatest number of taps (u (x)) was added to [20],[21]. The only element that matters for CRC and BCH encoding is the remainder r(x) [22],[23],[24]. The most significant coefficient is entered initially between the coefficients of u(x), and r(x) is found in the registers after the final coefficient of u(x) to be submitted. The data flow through the register is managed by the clock signal. Each flip-flop's data is moved to the next flip-flop in the register when the clock signal is high. The data inhe first flip-flop moves to the second flip-flop, the data in the second flip-flop moves to the third flip-flop and so on, making the data to "shift" through the register.

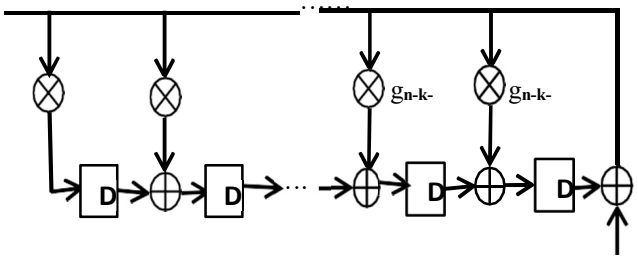
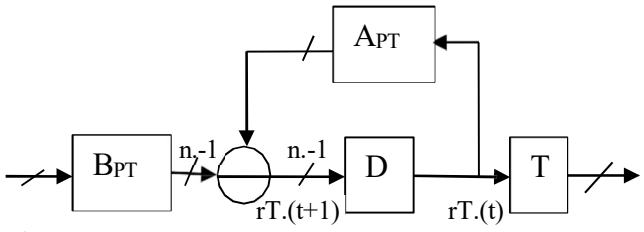


Figure 1: Architecture of serial LFSR. u(x)

It was suggested in [25], to change BpT and ApT, which are often known as the feedback and pre-processing matrices, to solve this issue. The values are as follows: up(t) = [u(t)... u(t+p-2), u(t+p-1)] and Bp = [Ap−1b…. Ab, b]. A p-parallel LFSR that modified p bits every clock cycle can be made using figure 2 displays a block schematic for building such a converted p-parallel LFSR. T has dimensions of (n − k) × (n − k), and as T increases, so does the complexity of the three matrix multiplications. From [26],[27] it turns out that the transformation also lowers the total gate count. In [3], a thorough search was conducted to identify the b1 that results in the least gate count. CMOS procedure A 1-XOR-gate that is exceptionally short [28]. becomes superfluous when 5 or 6 XOR gates fit inside a 1 ns delay an LFSR sequence can have a maximum the state vector as r(t) = T x rT (t) where, T is non-singular and is referred to as the transformation matrix. where,

$A_{PT} = T^{-1} \times A^{P} \times T$ $B_{PT} = T^{-1} \times B_P$



greatest number of bit patterns are produced by an LFSR and its maximal length is equal to 2^n-1 clock cycle.

$$g_0 \quad \begin{bmatrix} & & & \\ & & & \\ & & & \\ & & & \end{bmatrix}$$

$$A = \begin{matrix} g_{n-k-1} \\ g_{n-k-2} \\ \vdots \\ g_1 \\ g_0 \end{matrix} \begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ \vdots & \vdots & & \vdots \\ 0 & \dots & 0 & 1 \\ 0 & \dots & 0 & 0 \end{bmatrix}$$

COMPARISONS OF PARALLEL LFSRS

An almost complete collection of patterns and 2^n-1 clock cycle states may be achieved by an LFSR with suitable design. In this architecture, more intricate logic involving data inputs and register feedbacks generates the register inputs. To reduce the length of the data channel, a pipelining stage of width p is added. Therefore, in comparison to our approach, it requires p more delay elements (DEs). To the normalized area-time product (ATP), computed as (1.5 DE + XOR) CPD [1], is used to assess the efficiency of designs with various CPDs. In [7]'s architectural design, in a clock cycle, nearly all logic gates are active.

TABLE I COMPARISON OF PARALLEL LFSRS

Z	DESIGN	XOR	DE	CPD	ATP
CRC-12	[3]	113	35	5	827
	[7]	109	36	5	815
	[1]	103	24	4	695
	Proposed	101	22	4	536
CRC-16	[3]	187	48	5	1295
	[7]	113	50	5	940
	[1]	94	32	5	710
	Proposed	92	30	5	685
SDLC	[3]	207	48	5	1395
	[7]	139	50	5	1070
	[1]	97	32	3	435
	Proposed	95	31	3	425
CRC-16 Reverse	[3]	219	46	5	1440
	[7]	126	50	5	1005
	[1]	82	32	4	520
	Proposed	80	30	4	500
SDLC Reverse	[3]	217	48	5	1445
	[7]	127	50	5	1010
	[1]	90	32	4	552
	Proposed	85	31	4	526
CRC-32	[3]	968	96	5	5560
	[7]	794	96	5	4690
	[1]	675	64	5	3855
	Proposed	625	56	5	3545

n.-1

P n.-1

Figure 2: Architecture of parallel LFSR.

While the search is running, then remaining columns or rows are obtained via shifting modulo reduction. Rather, the objective is to reduce the weight of each row in BPT. When using SS [1], a matrix multiplication can be finished with fewer XOR gates, indicating that shared intermediate results for multiple outputs are calculated just once. Cycle 't' by r.(t) = [r.n−k−1(t), r.n−k−2(t) r.0(t)]. Let u.(t) be the input of clock cycle 't'. Then r. (t + 1) = A × r.(t) + b × u.(t) where, 'A' is companion matrix. The results of our comparison for the starting XOR gate count found. The suggested approach is contrasted with earlier ones and the outcome for various generating polynomials. The LFSR feedback function is usually represented by a characteristic polynomial. The

The number of XOR gates required to finish an operation may be calculated for an implementation by counting all of the 1s in the rows of the coupling matrices, deducting 1 from each row subtotal, and then computing the overall number of XOR gates. The input size is equal to the generator polynomial degree, r = n, in order to do an exhaustive search and reduce the hardware complexity of parallel retimed CRC computation systems. For n-bits CRC system's state space matrix was created in order to simplify the feedback loop. The suggested approach is contrasted with earlier ones and the outcome for various generating polynomials. where the number of delay elements is represented by DE. The findings show that my parallel architectures can produce hardware designs with the same CPD and the smallest XOR gates. To improve the data's interpretive qualities, the relative area time product values are listed using the suggested technique of normalization, in the rightmost column indicated by parenthesis. Throughout the experiment, we find that one object draws our attention. Our design can always obtain the best AT for various generator polynomials.

ute count. The setup and hold violations for the 4-bit LFSR investigated using the xilinx vivado tool. Timing violations: for a 4-bit LFSR, there are three with a slack of 0.230 ns. We calculated the static and dynamic power of 4bits, 8bits, 12bits, 16bits and 32bits LFSR using vivado tool. The transformation matrix is built using a parallel LFSR. As an efficiency metric, we define the area-time product (A.T.) as (C.P) (XOR + 1.5 D.E.), where 1.5 is the expected quantity of NAND gates that separate an XOR gate from a delay element. This is based on the notion that a delay element needs 6 2-input NAND gates, and an XOR gate needs 4 2-input NAND gates. For an LFSR generator with 32 bits of length and 16 steps at a time, implementation is preferable when the area time product of the price be less. We calculated the static and dynamic power of 4bits, 8bits, 12bits, 16bits and 32bits LFSR using vivado tool.

TABLE III
COMPARISON OF SERIAL LFSR

No. of Bits	Junction Temperature (ºC)	Effective thermal resistance (ºC/W)	Static power (w)	Dynamic power (w)	Total power (w)
4	33.6	2.5	0.091	1.444	1.535
5	33.6	2.5	0.091	1.761	1.852
8	33.6	2.5	0.091	2.712	2.803
12	33.6	2.5	0.091	3.906	3.997
16	33.6	2.5	0.091	5.267	5.358
32	33.6	2.5	0.091	10.545	10.636

TABLE II GENERATOR POLYNOMIALS

CODE	POLYNOMIALS
CRC-12	$x^{12}+x^{11}+x^3+x^2+x+1$
CRC-16	$x^{16}+x^{15}+x^2+1$
SDLC	$x^{16}+x^{12}+x^5+1$
CRC-16 Reverse	$x^{16}+x^{14}+x+1$
SDLC Reverse	$x^{16}+x^{11}+x^4+1$
CRC-32	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+$ x^4+x^2+x+1

Each generator polynomial's degree is taken into the parallelism level p. One acceptable matrix to show the efficiency of the area-time product (ATP) is given below.

ATP = (1.5 DE + XOR) CPD

Generator polynomials of CRC-16 reverse, this study [1] uses a greater total number of XOR gates than the findings in [7], but the CPD essentially stays the same. The overall no. of XOR gates use in CRC-32 is less in this study [1] than in the findings in [7], but the CPD essentially stays the same.

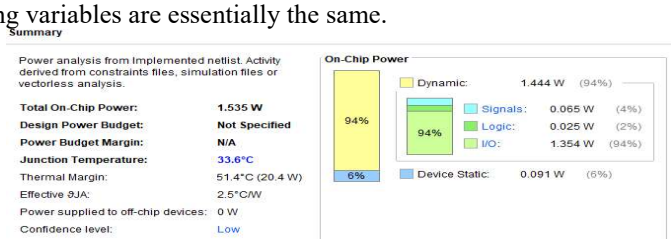
III. EXPERIMENTAL ANALYSIS

According to experimental data, the suggested architecture outperforms the recent architecture by as much as 55%. For an LFSR generator with 32 bits of length and 16 steps at a time, implementation is preferable when the area time product of the price be less. Schematic circuit diagram of 4 bits parallel LFSR as shown in figure 3, and RTL analysis shown in figure 4. The implementation is better when the A.T. value is lower. An ordinary 32-bit LFSR requires the construction of 32 D flip-flops. By using 4-bit flip-flops, 32-bit LFSR capabilities may be accomplished with less area, power consumption, and clock

BLE IV
COMPARISON OF PARALLEL LFSR

No. of Bits	Junction Temperature (ºC)	Effective thermal resistance (ºC/W)	Static power (w)	Dynamic power (w)	Total power (w)
4	33.6	2.5	0.091	3.902	3.993
5	33.6	2.5	0.091	3.812	3.903
8	33.6	2.5	0.091	7.111	7.202
12	33.6	2.5	0.091	12.133	12.224
16	33.6	2.5	0.091	12.620	12.711
32	33.6	2.5	0.091	28.165	28.256

. Thus, based on the findings from the experiment, the overall within-chip power appears to be growing sequentially with a variance of 3.99W. The variations are attributed to the worst hold and negative slack. Parallel designs for linear feedback shift registers reducing the feedback loop complexity of a parallel CRC transformation matrix and state-space transform. Comparing this design to previous designs, a significant reduced the power consumption is achieved without increasing in CPD. The input size is equal to the generator polynomial degree, r = n, in order to do an exhaustive search and reduce the hardware complexity of parallel retimed CRC computation systems. The remaining variables are essentially the same.



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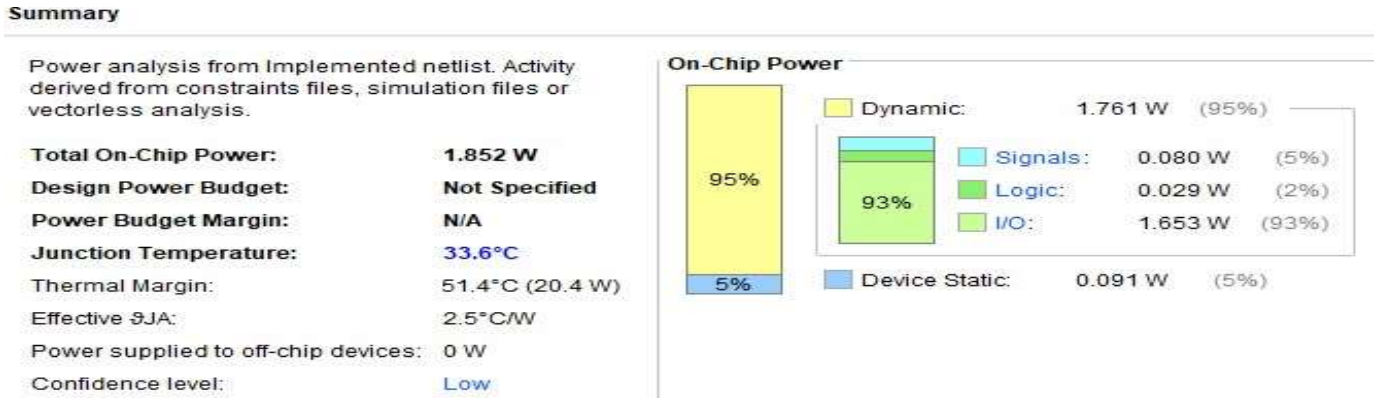

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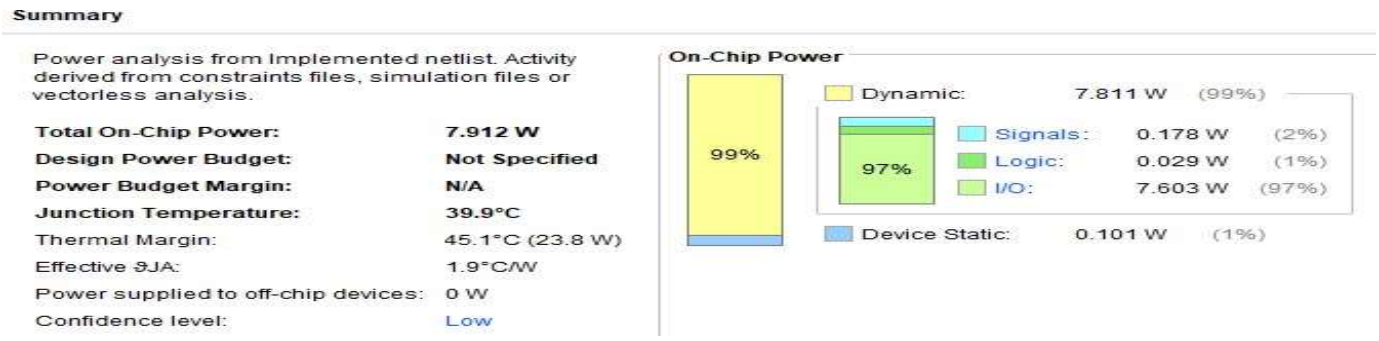

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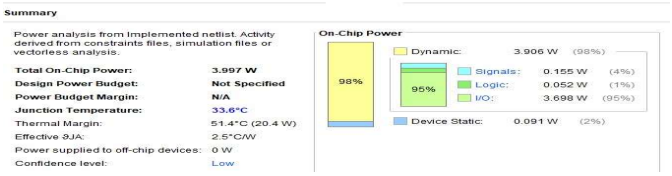

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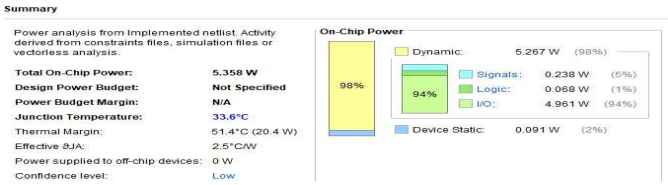

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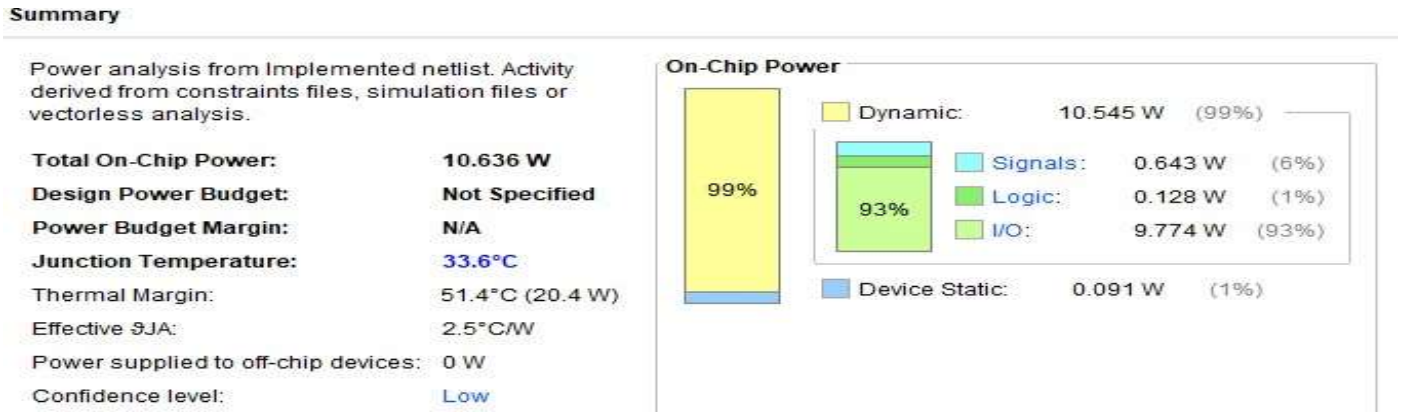
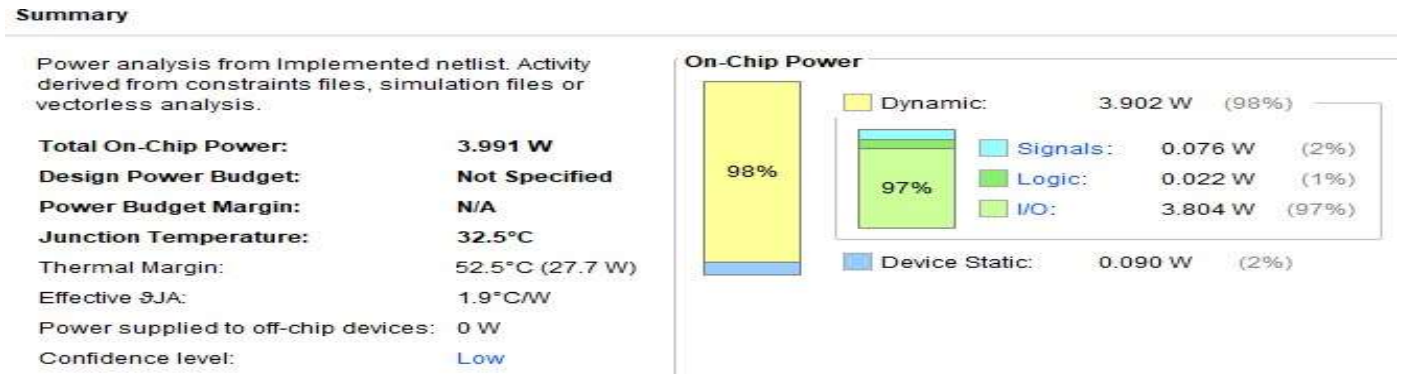


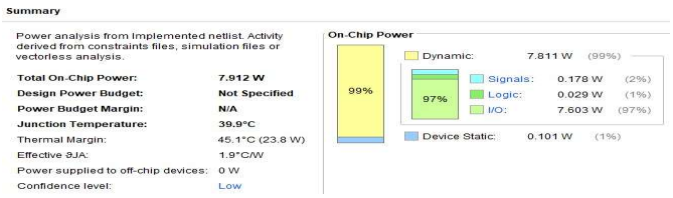
(f)

Figure 3: Power analysis of serial LFSR: (a) 4 bits (b) 5 bits (c) 8 bits (d) 12 bits (e) 16 bits (f) 32 bits.



(a)

(b)



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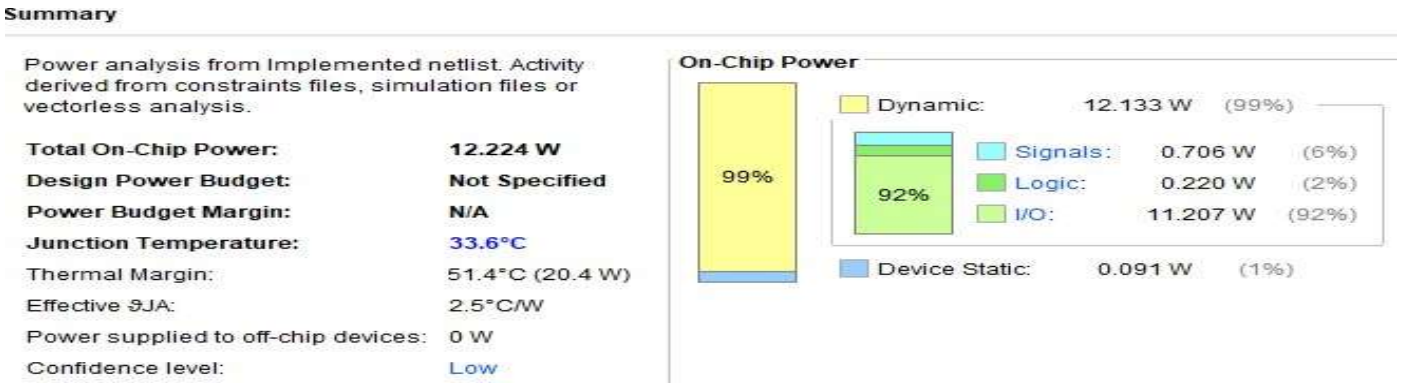

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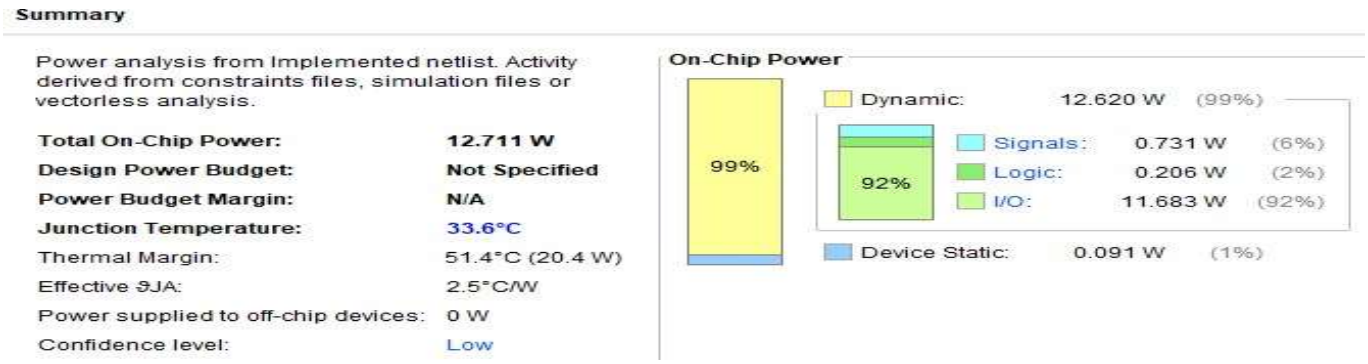

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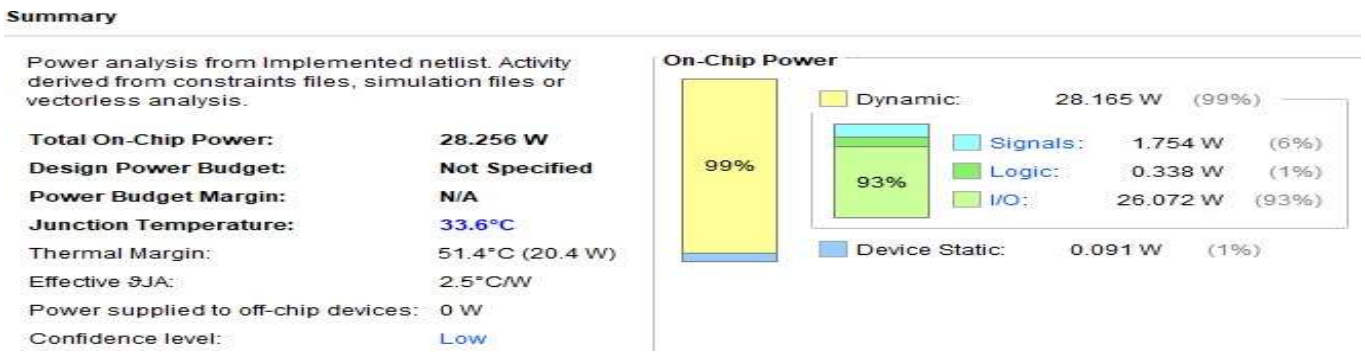

(f)

Figure 4: Power analysis of parallel LFSR: (a) 4 bits (b) 5 bits (c) 8 bits (d) 12 bits (e) 16 bits (f) 32 bits

IV. CONCLUSION

This paper presents the design of a multi-bit parallel and serial LFSR. Thus, based on the findings from the experiment, the overall within-chip power appears to be growing sequentially with a variance of 3.99W. The variations are attributed to the worst hold and negative slack. Parallel designs for linear feedback shift registers reducing the feedback loop complexity of a parallel CRC transformation matrix and state-space transform. Comparing this design to previous designs, a significant reduced the power consumption is achieved without increasing in CPD. The remaining variables are essentially the same. For n-bits CRC system's state space matrix was created in order to simplify the feedback loop. For CRC-32, 30% power and 6% gate count savings are achieved. Reduced size, power, and clock route count are achieved 4-bits flip-flops to accomplish 32-bit LFSR capability. With the help of the Xilinx Vivado Tool, violations for the 4-bits LFSR were examined.

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